a first surface upon which said bump electrodes are formed;

a second surface opposite said first surface;

a periphery adjacent said scribe lines;

a plurality of chip electrodes formed on said second surface along said periphery; and

a plurality of interconnection layers, each of said interconnection layers including a first end connected to a bump electrode of said bump electrodes and a second end connected a corresponding chip electrode of said chip electrodes,

each of said bump electrodes being located at a position other than over said corresponding chip electrode.

Please cancel claims 6-9 without prejudice or disclaimer.

10. (Twice Amended) A semiconductor wafer, including:

a plurality of chip sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes.

11. (Twice Amended) A semiconductor wafer, including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip

electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes.

Please add the following new claims:

--12. A semiconductor wafer as in claim 5, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum layer, wherein said plating contacts one of said bump electrodes and said aluminum layer contacts one of said chip electrodes.

13. A semiconductor wafer as in claim 12, wherein said plating comprises one of nickel and copper.

14. A semiconductor wafer as in claim 12, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

15. A semiconductor wafer as in claim 12, wherein said plating has a thickness of at least 5 micrometers.

16. A semiconductor wafer as in claim 12, further comprising a gold layer between said bump electrode and said plating.

17. A semiconductor wafer as in claim 5, wherein said semiconductor chip has a center and said interconnection layers extend from said periphery toward said center.

18. A semiconductor wafer as in claim 10, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum layer, wherein said plating contacts one of said bump electrodes and

said aluminum layer contacts one of said chip electrodes.

~~19~~ 5. A semiconductor wafer as in claim ~~18~~ 3, wherein said plating comprises one of nickel and copper.

~~20~~ 6. A semiconductor wafer as in claim ~~18~~ 3, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

~~21~~ 7. A semiconductor wafer as in claim ~~18~~ 3, wherein said plating has a thickness of at least 5 micrometers.

~~22~~ 8. A semiconductor wafer as in claim ~~18~~ 3, further comprising a gold layer between said bump electrode and said plating.

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~~23~~ 9. A semiconductor wafer as in claim ~~10~~ 1, wherein each of said chip sections has a center and a periphery and said interconnection layers extend from said periphery toward said center.

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24. A semiconductor wafer as in claim 11, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said plating contacts said bump electrode and said aluminum layer contacts said chip electrode.

~~25~~ 10. A semiconductor wafer as in claim ~~24~~ 4, wherein said plating comprises one of nickel and copper.

~~26~~ 11. A semiconductor wafer as in claim ~~24~~ 4, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

~~27~~ 12. A semiconductor wafer as in claim ~~24~~ 4, wherein said plating has a